

CLAIMS

We claim:

1. A method for fabricating a semiconductor component comprising:
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- a) forming a layer of dielectric over at least a portion of a passivation ledge in an emitter layer; and
 - b) overlapping a base contact onto the dielectric layer to form a semiconductor component.
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2. The method of claim 1 wherein the overlapping step further comprises overlapping the base contact onto the dielectric layer to substantially prevent exposure of the emitter layer and a base layer of the semiconductor component.
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3. The method of claim 2 wherein the overlapping step further comprises: etching away a region of the base layer and a region of a collector layer to form boundaries that are substantially aligned to a first edge of the base contact that is remote from the emitter layer.
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4. The method of claim 1 wherein the base layer is a p-type material.
5. The method of claim 1 wherein the dielectric material is selected from the group consisting of silicon nitride, aluminum nitride, silicon dioxide, silicon oxynitride and mixtures thereof.
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6. A method of fabricating a bipolar transistor comprising:
- a) providing a material structure comprising a subcollector layer, a collector layer, a base layer deposited over the collector layer, and an emitter layer having a surface passivation ledge disposed on the base layer;
 - b) forming a dielectric layer in the passivation ledge; and
 - c) overlapping a base contact onto the dielectric layer to form a bipolar transistor.
7. The method of claim 6 wherein the overlapping step further comprises overlapping the base contact onto the dielectric layer to substantially prevent exposure of the emitter layer and a base layer of the semiconductor component.
8. The method of claim 7 wherein the overlapping step further comprises: etching away a region of the base layer and a region of a collector layer to form boundaries that are substantially aligned to a first edge of the base contact that is remote from the emitter layer.
9. A method for fabricating a heterojunction bipolar transistor (HBT) comprising:
- a) providing a semiconductor device having a substrate layer, a subcollector layer, a collector layer, a base layer and an emitter layer, each layer formed on top of a preceeding layer;
 - b) etching the emitter layer to form an emitter mesa and a thin passivating ledge; and
 - c) depositing a metal layer on the base layer and the passivating ledge to form base contacts that are self aligned with respect to the ledge.

10007754-11501

10. A semiconductor component comprising:

- (a) a semiconductor substrate having an emitter layer, a base layer and a collector layer;
- (b) a dielectric layer formed over a passivation ledge in the emitter layer; and
- (c) a base contact disposed on the dielectric layer.

11. The semiconductor component of claim 10 wherein the dielectric layer is comprised of a material selected from the group consisting of silicon nitride, aluminum nitride, silicon dioxide, silicon oxynitride and mixtures thereof.

12. The semiconductor component of claim 10 wherein a region of the base layer and a region of the collector layer form boundaries that are substantially aligned to a first edge of the base contact that is remote from the emitter layer.

13. The semiconductor component of claim 10 wherein the base layer is comprised of a p-type material.

14. A heterojunction bipolar transistor (HBT) comprising:

- a) a substrate layer, a subcollector layer, a collector layer, a base layer and an emitter layer, each layer formed on top of the preceding layer;
- b) an emitter mesa and a thin passivating ledge formed in the emitter layer;
- c) base contacts deposited on the base layer wherein the base contacts are self aligned with respect to the passivating ledge.